Development of a Scalable Media-Processor System LSI based on the MISC, a Heterogeneous Multiprocessor SoC Platform

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Current System on a Chip (SoC) integrates custom hardwired logic together with a microprocessor (MPU) and/or a digital signal processor (DSP) into a single silicon. For example, MPEG4 codec engine is integrated with the MPU as the hardwired logic in order to boost the system performance. However, this approach is not sustainable because of increasing cost and cycle time of SoC development due to its complexity as well as possible changes in the data compression standard. Highly programmable and re-usable approach without using hardwired logic is, therefore, required for time and cost efficient SoC development.

Programmable solution is adaptive to emerging standards, new algorithms, different applications, and creating new applications with its flexibility. For example, still image processing employs multiple-standards, such as jpeg, jpeg2000, jbig, photo CD, wavelets. One programmable SoC solution is able to provide the solutions to this diverse standards.

In order to keep re-usability of a SoC, the platform based development approach is becoming crucial. It provides flexibility and scalability not only to software development, but also to hardware development.

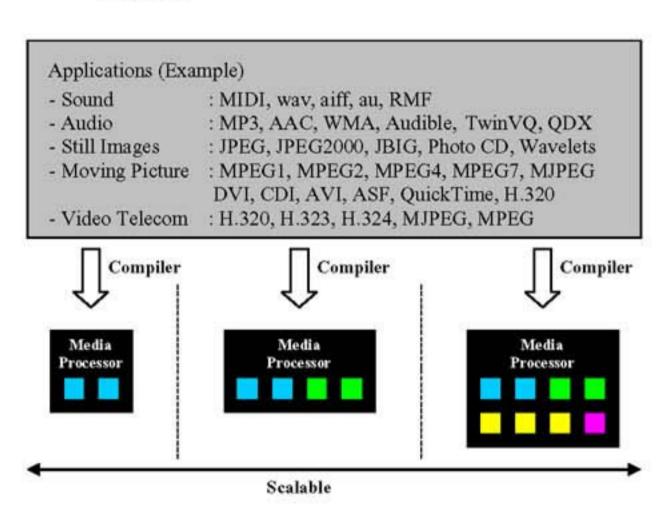
The MISC, Multiple Instruction Stream Computer, SoC platform IP developed by TOPS Systems, is a multi-processor based configurable platform. The MISC provides ease of applying and re-using the platform to a wide range of applications. Up to eight on chip heterogeneous processor engines not only provides ultimate data processing performance, provided software enables a precise dynamic power control. In addition to the flexibility the multi-processor platform provides, its virtual prototyping environment reduces time to market of the target application system.

MISC Platform I/O bus PU Penpheral Unit IM DM MI bus Master PU bus Controller Instruction Data Bus 32bit RISC Memory Memory D bus (128 bit) DE DE DE DE DSP DSP DSP DSP RISC RISC RISC RISC Engine Engine Engine Engine Engine Engine Engine Engine 32bit MAC 32bit MAC

The goal of this project is to develop the Scalable Media-Processor System providing following features.

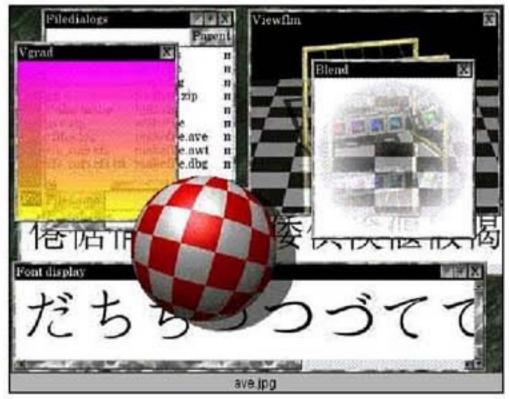
< Features of Scalable Media-Processor >

- Fully programmable by software
- Easily scalable by combination of heterogeneous and multiple media-data processing engines
- High performance by parallel processing
- Dynamic power and performance control by software



In this project, the MISC platform IP is used as a base architecture, and the following items will be developed to build a multi-media system.

- Media-data processing engines
- C compiler for Media-data processing engines
- Multi-Media application software utilizing heterogeneous parallel processing
- Scalable Media-Processor System LSI
- Demonstration System



Screen image (presented by Tao Group)