A Programmable Low-power Matched Filter using Charge-Domain Signal Processing

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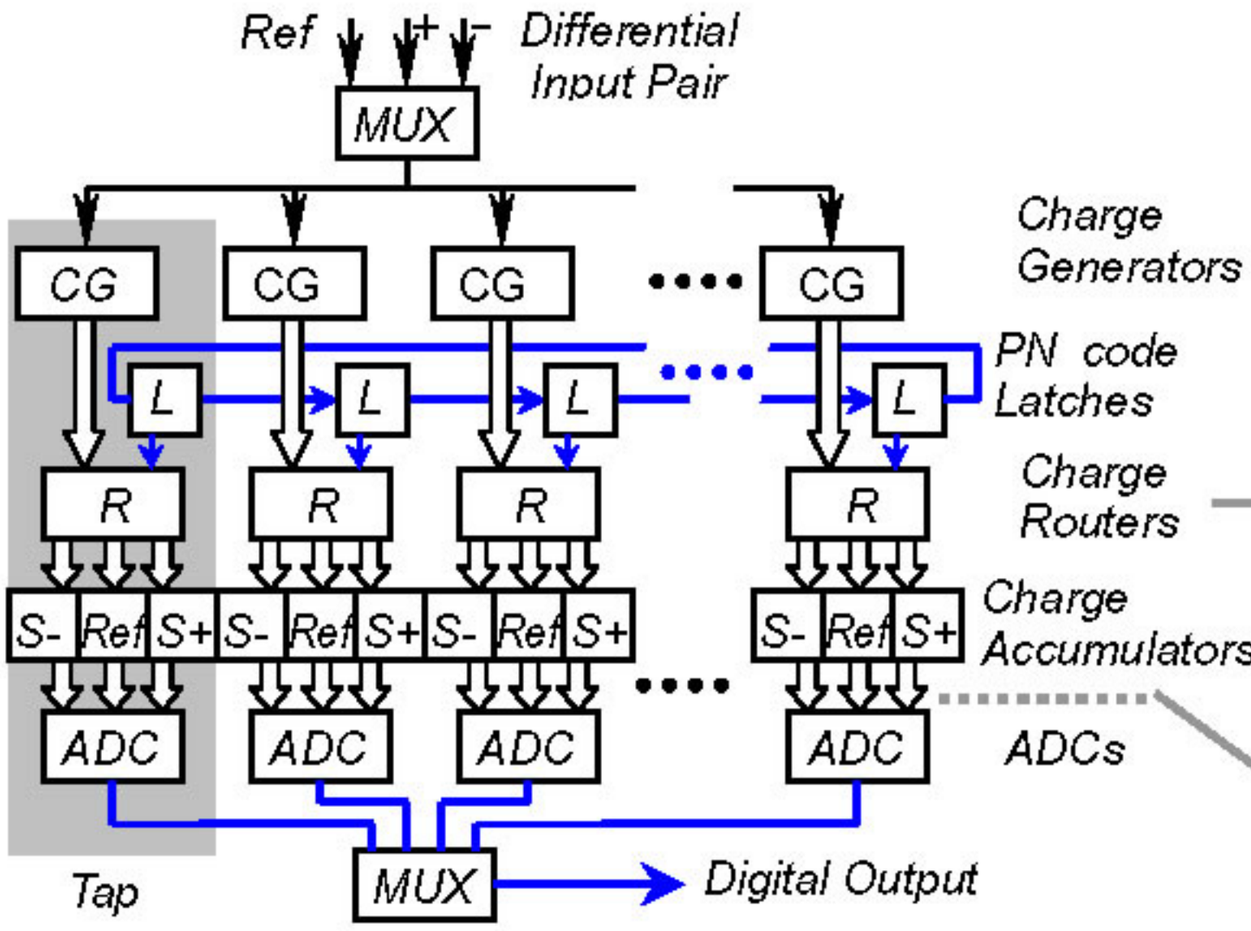

Fig.A Transposed FIR Matched-Filter with PN Re-circulation
(US.Patent 5,936,567; JP3069637)

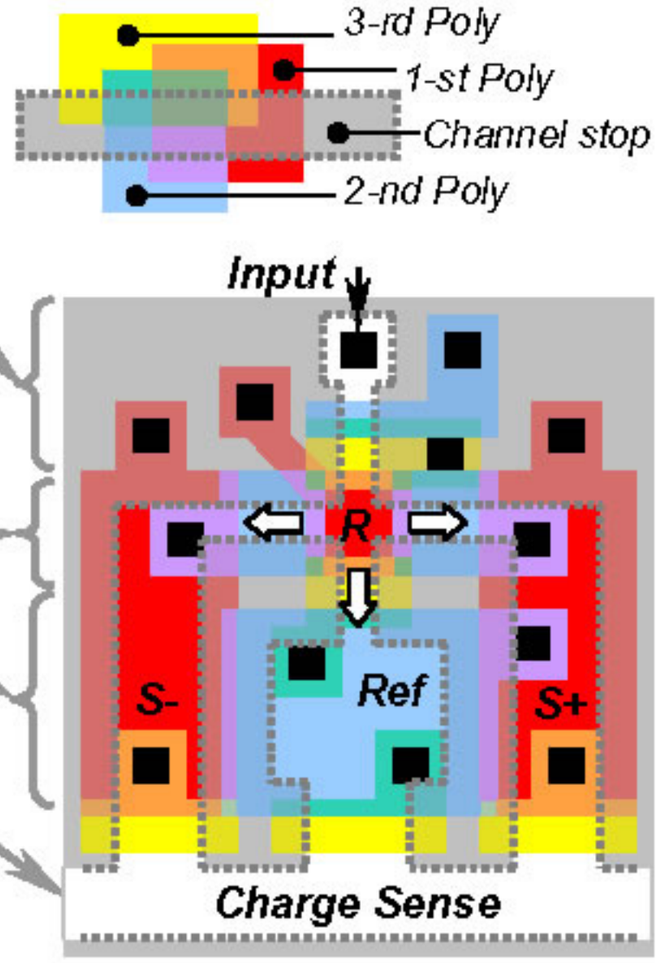

Fig.B Schematic drawing of CCD portion for each tap

Introduction

The acquisition of PN-code timing is very important process in the CDMA communications to demodulate received signal into base-band signal. Although the operation can be realized ideally by the introduction of matched filter (MF), the device has not so widely been used yet because of additional cost and power consumption, especially for mobile communication devices.

In this poster we propose a new MF architecture "transposed form FIR with PN-re-circulation" which is thought to operate with significantly low power consumption.

Device Structure

This MF has "full-correlator bank (FCB) structure" which consists from an array of many independent receivers. (Fig.A) And each receiver in the array contains a charge generator, a charge packet router (*i.e.* 1-bit multiplier) and three charge accumulators all operate in charge-domain (Fig.B), being controlled by digital logic control circuits. This simple structure enjoys the merits of charge domain processing described below:

- "Feed-through-free" switching by charge routing.
- Accurate and compact addition by charge binning.

The FCB-MF requires no transversal shift-register unlike conventional transposed FIR filters. In the FCB-MF, a set of charge accumulators are used for the integration of correlation result, instead of analog shift register which operates under sampling rate of input signal dissipating large amount of power.

The FCB-MF suffers from the inherent problem of non-uniformity among taps, which is caused by its basic structure to compose single correlation output all from signal supplied by the same tap components.

We use AD converter as a signal divider to overcome this problem by canceling common deviation factor included in both of input signal (dividend) and reference signal (divider).

Estimated Power Dissipation

The power dissipation of FCB-MF device under this plan is estimated as low as 0.16 (μW/MHz/tap) which corresponds to 1/20~1/30 of recent low-power mixed signal MFs.

Table 1. Comparison of Power Dissipation at MFs

Manufacturer	Process	Topology **	Power ***	Ratio
I. 1996	CMOS	Direct	32.4	100 *
II. 2001	CMOS	FCB	[4.61]	14.2*
GDS (proposed)	CMOS/CCD	FCB	0.16	0.5

* : measured data **: all with PN-code re-circulation
*** : unit in (μW/MHz/tap), power without ADC
[ ] : Estimated Data

Another Merits of this MF

- ***Capability for higher operation rate.***
  Very short charge transfer channel enables to raise clock rate of this device allowing degradation of charge transfer efficiency.
- ***Scalability.***
  Theoretically, no limitation is there to expand tap number.
- ***Re-configurability.***
  Each tap of this MF is independent correlator, therefore any combination is possible by the configuration of input and output connection. (long MF, short MFs, multi-bit MF, etc.)

Technological Challenges

The clock signals required to drive this device are far complicated compared with CCD imagers, so that it seems to be very difficult to supply clock signal from external logic circuits.

Therefore, CMOS/CCD process is necessary for the production of this device.