Low Power Circuit Technology of Microcontrollers

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Introduction

Low power dissipation of the microcontrollers is key feature to today's and future personal systems such as cellar phones and wearable computers, because they need high performance with long battery life.

Three low power circuit schemes has been developed. These schemes achieve not only super low power data retention but low voltage operation without sacrifice of high performance.

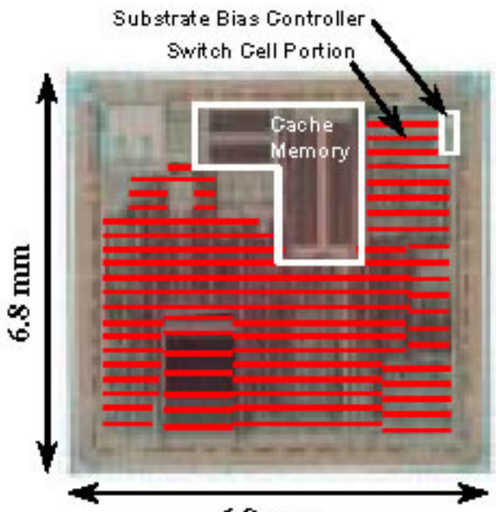

Figure 1 Chip microphotograph of low power microcontroller that achieves 18μA data retention, 200MHz operation, and 1000MIPS/W

Low Power Circuit Schemes

(1) Low Power in Data Retention Mode(Fig.2, ref.2)

Feature:
Deep substrate bias is applied with reducing supply voltage so that GIDL(Gate Induced Drain Leakage) current is not increased.
Effect:
The current in data retention mode is decreased to 1/76 .

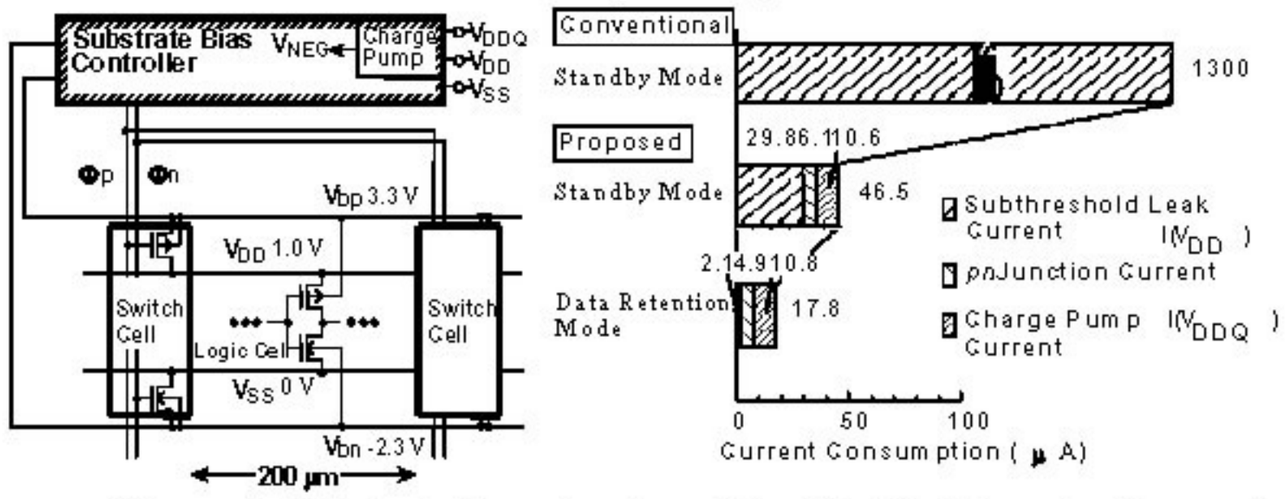

Figure 2 Substrate bias circuit and its effect in data retention mode.

(2) Low Power in Logic Circuits (Fig.3, ref.3)

Feature:
Controlled substrate bias is dynamically applied in operation mode so that delay of logic circuit becomes constant.
Effect:
Performance variation is decreased to ¼ of conventional value at 0.9V .

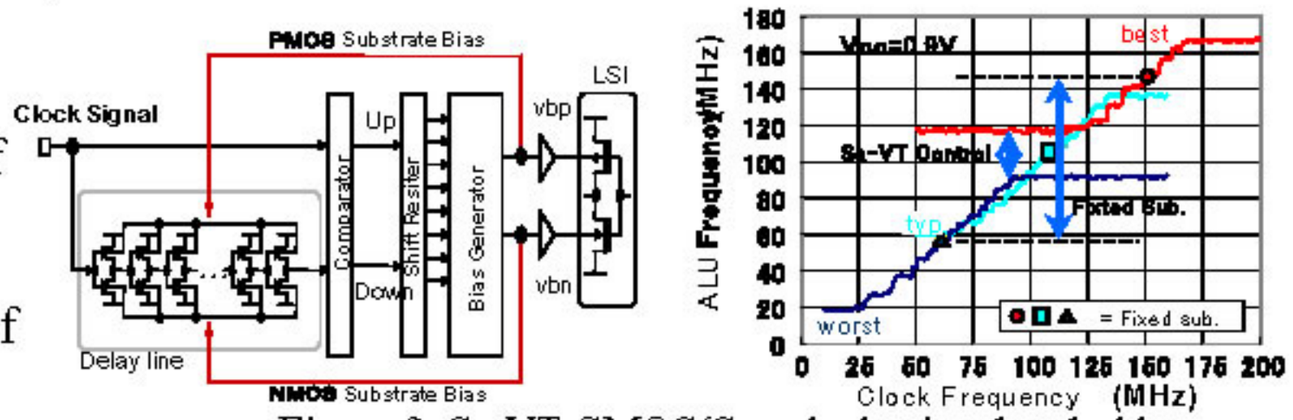

Figure 3 Sa-VT CMOS(Speed adaptive threshold voltage) circuit and its effect at 0.9V supply voltage.

(3) Low Power in Memory Arrays (Fig.4, ref.4)

Feature:
Symmetric layout memory cell and plural dummy memory cell circuit enables high speed and low voltage operation of SRAM array.
Effect:
Power of cache memory at 120MHz is decreased to 1/300 of that at 1GHz

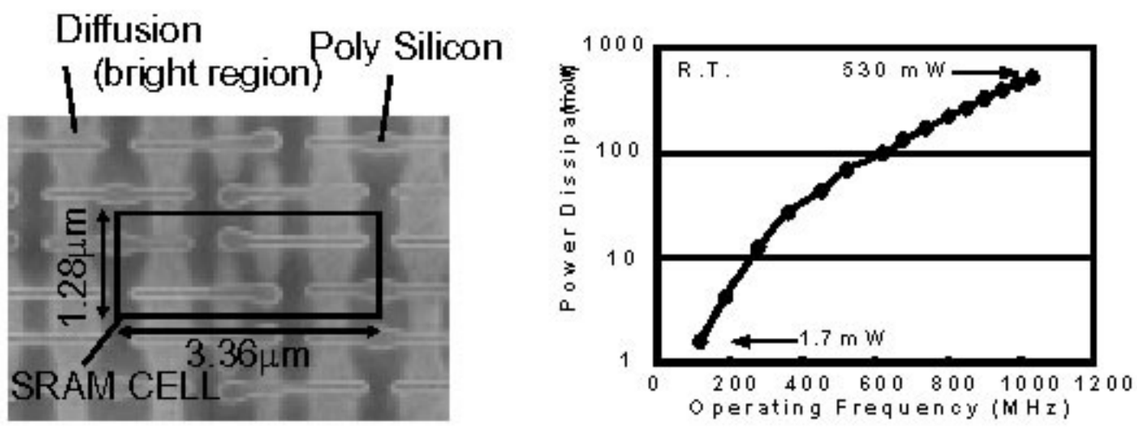

Figure 4 Symmetry memory cell and power of 256kbit array using this memory cells

Future Plan

A part of this research is practical level(ref.1). We will further reduce the operating voltage to sub 0.5V, and realize ultra low power microcontroller within five years.

References

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2) H. Mizuno et al, "A 18-μA Standby Current 1.8-V 200-MHz, Microprocessor with Self Substrate-Biased Data Retention Mode", 1999 ISSCC, 16.4
3) M. Miyazaki et al., "A 1000-MIPS/W Microprocessor using in Speed-Adaptive Threshold-Voltage CMOS with Forward Bias", 2000 ISSCC, 25.6.
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