On a New Type of Programmable Logic Devices and Their Logic Synthesis

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1 Introduction

As the minimum dimensions of LSI decrease, we can only afford to synthesize into regular structures. Since manufacturing variations will be so severe, custom design circuits will be too difficult to get right. Effects like cross-talk noise, inductive effects, and delay prediction will grow beyond the complexity bound for economical custom design.

A regular structure is one that involves a repeated pattern, and has the following desirable features:

- Resistive to the environment and production variations.
- Easy to expand.
- Easy to reprogram.
- Easy to make fault tolerant by adding redundancy and by using error detection and correction technique.

2 Objective of Research

To develop a new programmable logic device having regular structure, and analyze their speed, area and power dissipation. Also to develop their logic synthesis system.

3 LUT Cascade Method

In this research, we will consider the lookup table cascade method [1]. In the LUT cascade method,

- The logic function is represented by a cascade of LUTs (Fig. 1).
- The LUTs are implemented by a ROM/RAM.
- The interconnections are implemented by a programmable sequential control circuit (Fig. 2).

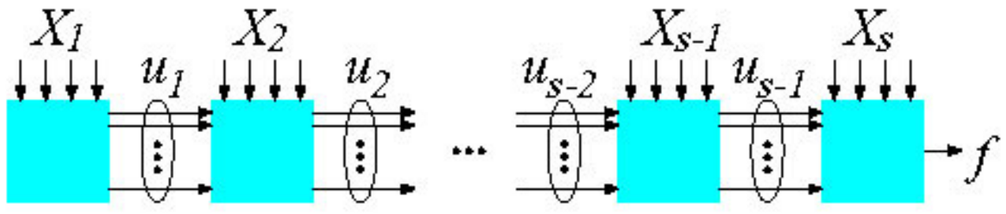

Figure 1: LUT Cascade.

In the LUT cascade method, the interconnection problem is minimized, and the major problems are reduction of logical levels and reduction of ROM/RAMs. Preliminary experiments show that LUT cascade method is about ten times faster than conventional branching program. The following

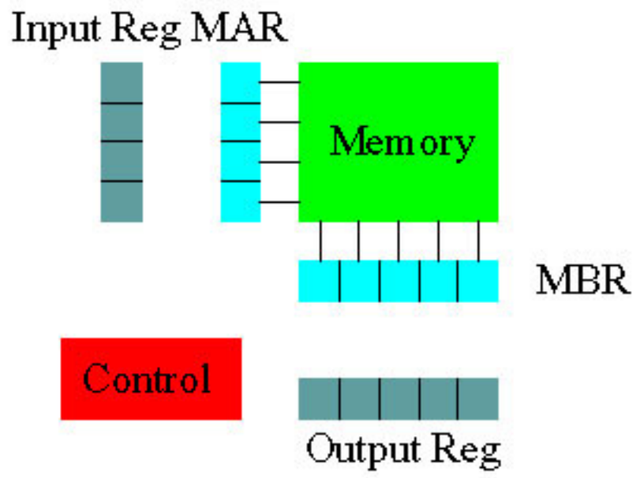

Figure 2: Architecture.

Table 1: Comparison of Programmable Logic Devices.

	Speed	Area	Design Cost
ROM/RAM	High	Too large	Small
FPGA	High	Medium	Medium
LUT cascade	Medium	Medium	Small
ROM+ MPU	Low	Medium	Small

table compares these methods. The LUT cascade method is not so fast and low power as custom logic circuits, but faster and dissipate lower power than software implemented by the conventional microprocessors. In the LUT cascade method, we can

- Minimize the interconnection problem.
- Increase parallelism by utilizing multiple-bits of memory.
- Reduce the size of memory by "bit packing" technique and encoding technique of ECFN.
- Control the size and speed according to the available memory.

Although, the LUT cascades are universal, it is not so efficient to implement all the system by LUT cascades. In the practical applications, we can combine with other methods: ROM, RAM, PLA, FPGA and MPU.

References

[1] T. Sasao, M. Matsuura and Y. Iguchi, "A cascade realization of multiple-output function for reconfigurable hardware, "International Workshop on Logic and Synthesis (IWLS-2001), Lake Tahoe, CA, June 12-15, 2001. http://www.lsi-cad.com/sasao/Papers/pub2001.html