Development of an optically reconfigurable gate array (ORGA) and implementation of a reconfigurable processor

光再構成型ゲートアレイの開発と再構成型プロッセッサの実装

Kyushu Institute of Technology * , Shizuoka University **

Minoru Watanabe *, Fuminori Kobayashi *, Junji Ohtsubo **, Taiichi Otsuji *

九州工業大学 *, 静岡大学 **, ○* 渡邊 実, *小林史典, **大坪順次, *尾辻泰一

1. Development of an optically reconfigurable gate array (ORGA)

Hardware implementation of software is expected to improve processing speed for real-time application (e.g., image processing, image compression or decompression, high speed communication). However, available Application Specific Integrated Circuits (ASICs) can only provide fragment functions of the software due to the circuit scale of the ASICs.

Reconfigurable hardware using Field Programmable Gate Arrays (FPGAs) has been focused on taking advantage not only of the processing speed but also of configurable and reconfigurable capabilities like software. However, the configuration of the FPGAs requires long time delays and the FPGAs must sit idle while it is being reconfigured. Therefore, a conventional reconfigurable system can not fully exploit the flexibility offered by reconfigurable hardware.

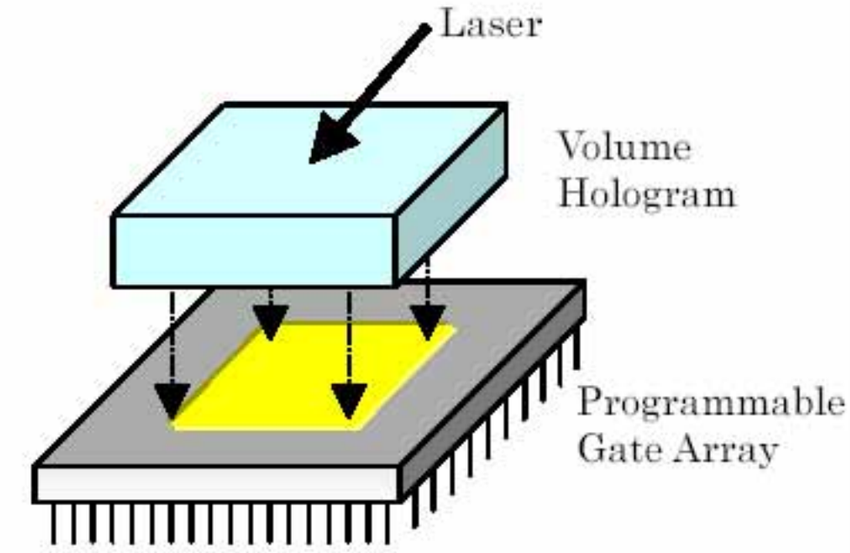

Fig.1. Conceptual block diagram of an optically reconfigurable gate array .

In this scheme, an optically reconfigurable gate array (ORGA) is developed to overcome the slow configuration time. The conceptual block diagram of the ORGA is illustrated in Fig.1. The configuration data stored in a volume hologram is written optically in a 2D onto each of the on-chip photodetectors of the programmable gate array. As the result, the ORGA can achieve very fast parallel configuration and reconfiguration.

2. Implementation of a reconfigurable processor on an ORGA

A reconfigurable processor on an ORGA enables us to implement almost of a current computer system into an ORGA as shown in Fig.2. Each conventional general purpose unit is disassembled into various small function elements. The small functions necessary in a clock cycle can be implemented into a portion of the logic resource of the ORGA. High processing speed can be achieved, since the functions can be massibly implemented into the ORGA.

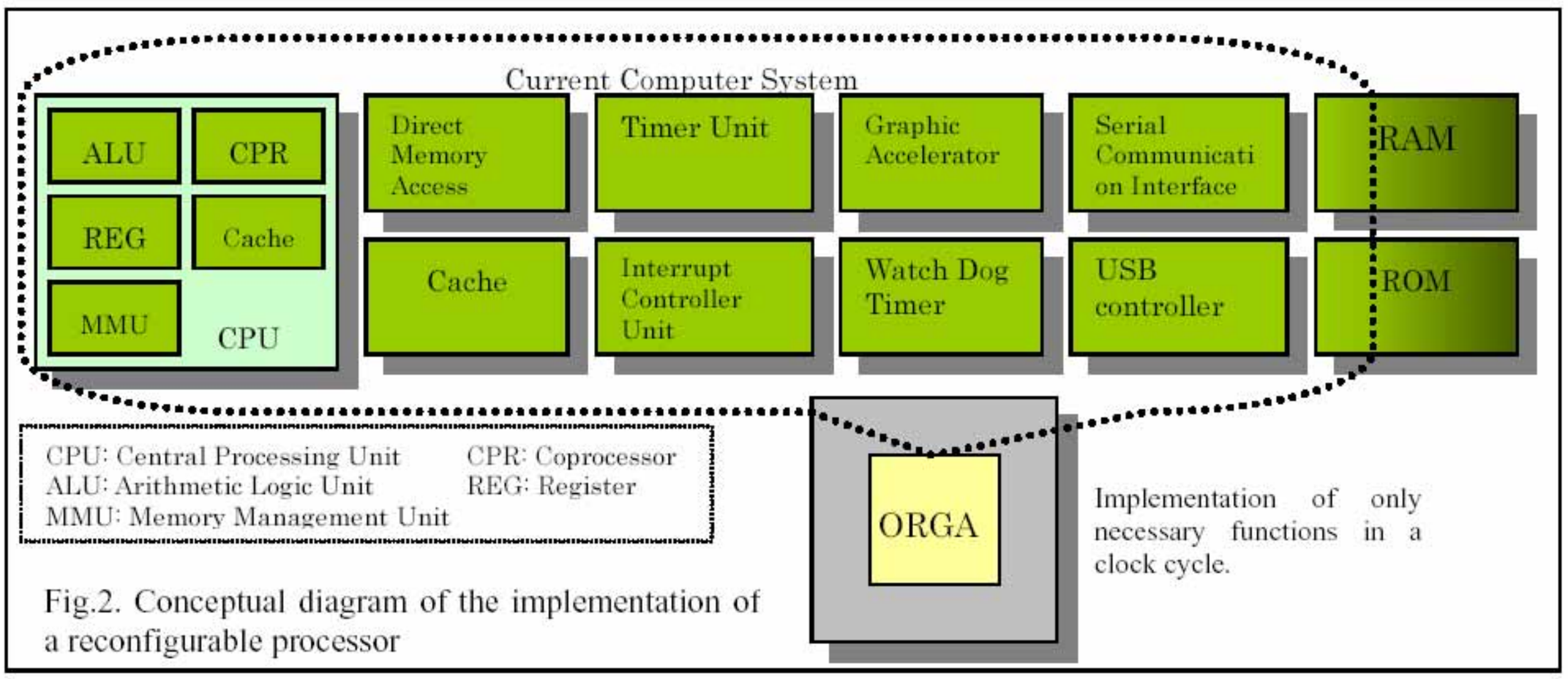

Fig.2. Conceptual diagram of the implementation of a reconfigurable processor